Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. **(previously presented):** A pipeline memory device comprising:

a plurality of memory cells that store data;

a data transfer path on which the data is transferred;

a data fetching control circuit configured to generate a first pipeline control pulse signal and a second pipeline control pulse signal;

a first pipeline stage that latches the data on the data transfer path in response to pulses of the first pipeline control pulse signal;

a second pipeline stage that latches the data latched by the first pipeline stage in response to pulses of the second pipeline control pulse signal; and

a third pipeline stage that outputs the data latched by the second pipeline stage to a data output pad in response to a data output clock signal,

wherein an initial pulse of the second pipeline control pulse signal is delayed relative to an initial pulse of the first pipeline control pulse signal, and

wherein a pulse width of at least the initial pulse of the second pipeline control pulse signal is less than a pulse width of each of the pulses of the first pipeline control pulse signal.

2. **(previously presented):** The pipeline memory device of claim 1, wherein the data fetching control circuit comprises:

a first edge trigger delay circuit that receives a first clock signal and generates the first pipeline control pulse signal; and

a multiplexer that receives a second clock signal and the first pipeline control pulse signal, and generates the second pipeline control pulse signal.

3. **(previously presented):** The pipeline memory device of claim 2, wherein the first edge trigger delay circuit comprises an even number of inverters in a chain.

4. **(previously presented):** A pipeline memory device comprising:

a plurality of memory cells that store data;

a data transfer path on which the data is transferred;

a data fetching control circuit that is configured to generate a first pipeline control signal in response to a first clock signal for generating the first pipeline control signal, and a second pipeline control signal in response to both a second clock signal for generating the second pipeline control signal and the first pipeline control signal;

a first pipeline stage that latches the data on the data transfer path in response to the first pipeline control signal;

a second pipeline stage that latches the data latched by the first pipeline stage in response to the second pipeline control signal; and

a third pipeline stage that outputs the data latched by the second pipeline stage to a data output pad in response to a data output clock signal;

wherein the data fetching control circuit comprises:

a first edge trigger delay circuit that receives the first clock signal for generating the first pipeline control signal and generates the first pipeline control signal;

a second edge trigger delay circuit that receives the second clock signal for generating the second pipeline control signal;

a first inverter that inverts the first pipeline control signal;

a NAND gate that receives the output of the first inverter and the second edge trigger delay circuit; and

a second inverter that inverts the output of the NAND gate to output the second pipeline control signal.

5. **(previously presented):** The pipeline memory device of claim 4, wherein the first and second edge trigger delay circuits comprise an even number of inverters in a chain.

6. **(previously presented):** A data fetching method for a pipeline memory device, comprising:

transferring data stored in memory cells along a transfer path;

generating a first pipeline control pulse signal in response to a first clock signal;

generating a second pipeline control pulse signal in response to a second clock signal and the first pipeline control pulse signal;

latching the data to a first pipeline stage on the transfer path in response to pulses of the first pipeline control pulse signal;

latching the data to a second pipeline stage on the transfer path in response to pulses of the second pipeline control pulse signal; and

outputting the data from the second pipeline stage to a data output pad in response to a data output clock signal,

wherein an initial pulse of the second pipeline control pulse signal is delayed relative to an initial pulse of the first pipeline control pulse signal, and

wherein a pulse width of at least the initial pulse of the second pipeline control pulse signal is less than a pulse width of each of the pulses of the first pipeline control pulse signal.

7. **(cancelled)**

8. **(currently amended):** The method of claim [[7]] 6, wherein the pulses of the second pipeline control pulse signal do not overlap the pulses of the first pipeline control pulse signal.

9. **(previously presented):** An apparatus comprising:

at least one memory cell;

a first pipeline stage coupled to the output of the at least one memory cell, wherein the first pipeline stage is driven by a first control pulse signal; and

a second pipeline stage coupled to the output of the first pipeline stage, wherein the second pipeline stage is driven by a second control pulse signal,

wherein an initial pulse of the second control pulse signal is delayed relative to an initial pulse of the first control pulse signal, and

wherein a pulse width of at least the initial pulse of the second control pulse signal is less than a pulse width of pulses of the first control pulse signal.

10. **(previously presented):** The apparatus of claim 9, wherein the first control pulse signal and the second control pulse signal are driven by a clock signal.

11. **(original):** The apparatus of claim 10, wherein the clock signal is an internal clock signal.

12. **(currently amended):** The apparatus of claim 10, wherein each pulse of the first control pulse signal is delayed relative to each pulse of the clock signal by a first delay; and

wherein [[each]] an initial pulse of the second control pulse signal is delayed relative to [[each]] a second pulse of the clock signal by a second delay.

13. **(original):** The apparatus of claim 12, wherein the first delay is larger than the second delay.

14. **(previously presented):** The apparatus of claim 9, wherein the pulses of the first control pulse signal do not overlap the pulses of the second control pulse signal.

15 – 16. **(cancelled)**

17. **(previously presented):** The apparatus of claim 1, wherein the data fetching control circuit comprises a first circuit which generates the first pipeline control pulse signal, and a second circuit which generates the second pipeline control pulse signal,

wherein first circuit of the data fetching control circuit receives a first clock signal and outputs the first pipeline control pulse signal in accordance with the first clock signal, and

wherein the second circuit of the data fetching control circuit receives a second clock signal and the first pipeline control pulse signal, and outputs the second pipeline control pulse signal in accordance with the second clock signal and the first pipeline control pulse signal.